User's Guide

AVCLVCDIRCNTRL-EVM Evaluation Module

ABSTRACT

This user's guide describes the characteristics, operation, and use of the AVCLVCDIRCNTRL-EVM evaluation module built for the direction controlled translation devices. A complete printed-circuit board layout, schematic diagram, and bill of materials are included in this document.

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Trademarks

1 Introduction

The AVCLVCDIRCNTRL-EVM helps evaluate the operation of the devices belonging to the direction controlled translation device family.

1.1 Features

Direction controlled translators allow the designer to configure the direction of data flow through the use of one or more direction control pins. These translators are designed for push-pull IOs. The three families of general purpose translators in the direction controlled portfolio are the AXC, AVC and LVC. Additionally, there are the AXCH, LVCH and AVCH translators, which are functionally equivalent to their AXC, LVC and AVC counterparts with the exception of the inclusion of bus-hold circuits on the I/O lines. The bus-hold circuit will maintain the last logic state seen on the inputs when the bus is in a high impedance state, preventing the negative effects of floating CMOS inputs and eliminating the need for external pull-up or pull-down resistors in cases where the inputs cannot be held at a defined state by an external driver. Note that the control inputs do not have the bus-hold circuitry and only the data I/O ports do. Refer to the application note on bus hold circuits for more information. Table 1-1 shows a generic comparison between AXC, AVC and LVC families. The physical board is shown in Figure 1-1. Note that the actual orderable EVM do not have devices populated.

Table 1-1. AXC, AVC and LVC Comparison

Parameter	AXC	AVC	LVC
Operating Range	0.65 V to 3.6 V	1.2 V to 3.6 V	1.65 V to 5.5 V
Drive Strength per Channel	12 mA	12 mA	32 mA
Icc Quiescent Current(1T)	6 uA	20 uA	6 uA
Input Leakage Current	1 uA	1 uA	2 uA
Max Data Rate(1T)	up to 500 Mbps	up to 500 Mbps	up to 420 Mbps
t_{PD} (1.8/3.3VccAB @15pF)	4 ns / 4 ns	3.4 ns / 4.4 ns	8.3 ns / 15.5 ns

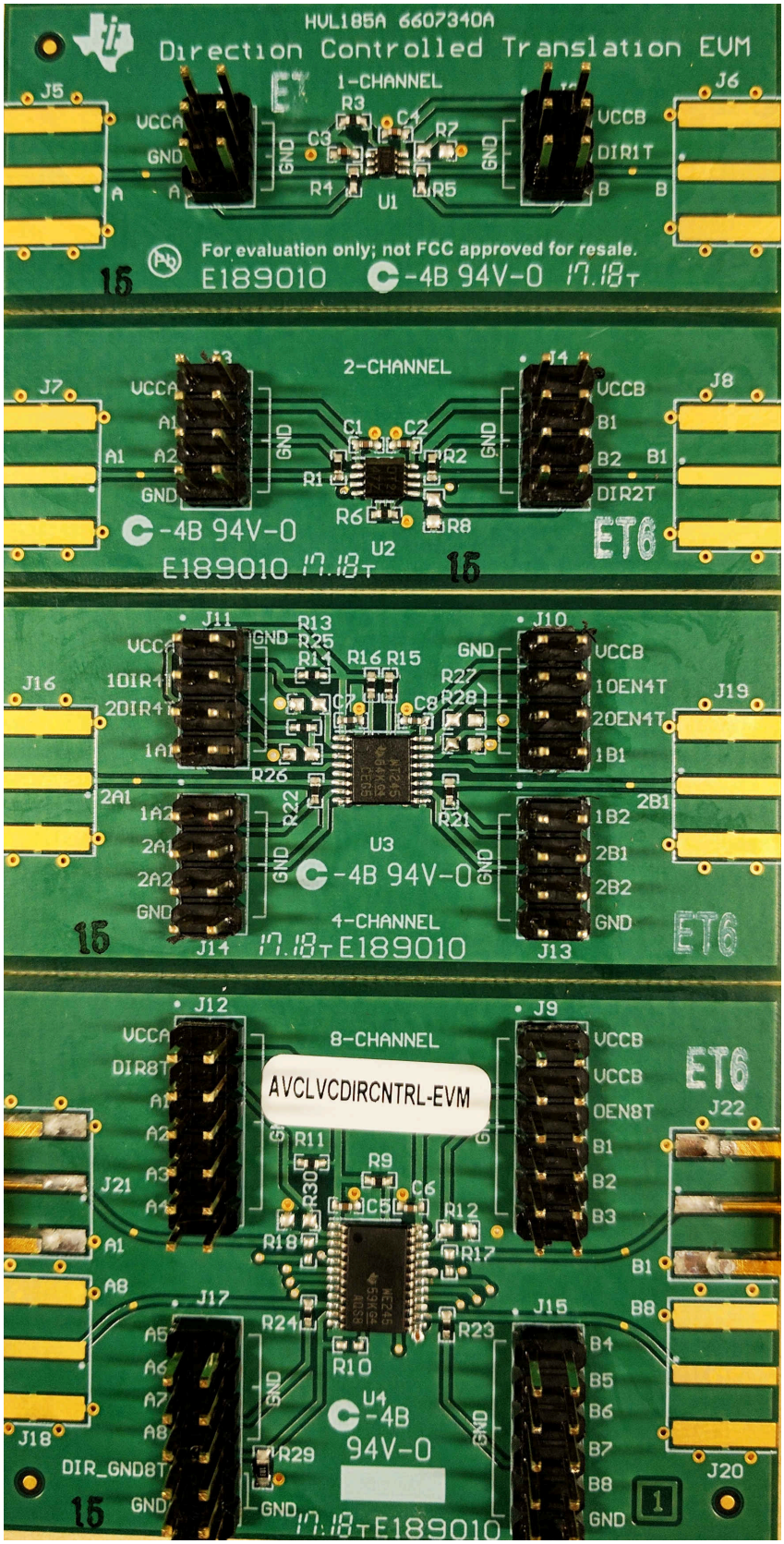

Figure 1-1. SN74XVCXTX45EVM: 8, 4, 2, 1 Channel versions

The various packages which the EVM supports are listed in Table 1-2.

Table 1-2. EVM Package Options

Version	Package	Device Populated
One Channel	DCK	No
Two Channel	DCT	No
Four Channel	PW	No
Eight Channel	PW	No

The AVCLVCDIRCNTRL-EVM is built as a multi-purpose EVM to support all the devices listed in Table 1-3. The LVCC device family has pin 23 as NC(No Connect) instead of V_{CCB}

Table 1-3. Supported Devices

	Supported Devices	Order Samples
One Channel	SN74AXC1T45	SN74AXC1T45 samples
	SN74AXC1T45-Q1	SN74AXC1T45-Q1 samples
	SN74AXCH1T45	SN74AXCH1T45 samples
	SN74AVC1T45	SN74AVC1T45 samples
	SN74AVCH1T45	SN74AVCH1T45 samples
	SN74LVC1T45	SN74LVC1T45 samples
	SN74LVC1T45-Q1	SN74LVC1T45-Q1 samples
Two Channel	SN74AVC2T45-Q1	SN74AVC2T45-Q1 samples
	SN74AVC2T45	SN74AVC2T45 samples
	SN74AVCH2T45	SN74AVCH2T45 samples
	SN74LVC2T45-Q1	SN74LVC2T45-Q1 samples
	SN74LVC2T45	SN74LVC2T45 samples
Four Channel	SN74AXC4T245	SN74AXC4T245 samples
	SN74AXCH4T245	SN74AXCH4T245 samples
	SN74AVC4T245	SN74AVC4T245 samples
	SN74AVCH4T245	SN74AVCH4T245 samples
	SN74AVC4T245-Q1	SN74AVC4T245-Q1 samples
Eight Channel	SN74AXC8T245	SN74AXC8T245 samples
	SN74AXCH8T245	SN74AXHC8T245 samples
	SN74AXC8T245-Q1	SN74AXC8T245-Q1 samples
	SN74AVC8T245	SN74AVC8T245 samples
	SN74AVCH8T245	SN74AVCH8T245 samples
	SN74AVC8T245-Q1	SN74AVC8T245-Q1 samples
	SN74LVC8T245	SN74LVC8T245 samples
	SN74LVCH8T245	SN74LVCH8T245 samples
	SN74LVC8T245-Q1	SN74LVC8T245-Q1 samples
	SN74LVCC3245A	SN74LVCC3245A samples
	SN74LVCC4245A	SN74LVCC4245A samples

1.2 Hardware Description

1.2.1 Headers

The EVM has standard 100-mil headers with the side closer to the device connected to ground. The side farther away from the device is mapped to the device pinout for easier connection as seen in Figure 1-1. The silkscreen indicates the pin function.

1.2.2 Bypass Capacitors

C1, C3, C5, and C7 are the bypass capacitors for V_{CCA} while C2, C4, C6, and C8 are the bypass capacitors for V_{CCB} ,each with a value of 0.1 µF.

1.2.3 Pullup and Pulldown Resistors

The direction control and output enable pins are the inputs for the devices and should never be left floating. The CMOS inputs must be held at a known state, either V_{CC} or ground, to ensure proper device operation. Refer to *Implications of Slow or Floating CMOS Inputs* (SCBA004). The default state in the EVM is referenced to V_{CCA} using a 10-kΩ pull-up resistor. There is also the option of connecting the inputs to ground using pull-down resistors, or directly to ground via jumper on the header pins.

Table 1-4 lists the 10-kΩ pullup and pulldown resistors.

Table 1-4. Pullup and Pulldown Resistors

Device	Pin	Pullup (10-kΩ)	Pulldown(10-kΩ)
One Channel(1)	DIR	R3	R7
Two Channel(2)	DIR	R6	R8
Four Channel(3)	DIR1	R13	R25
	DIR2	R14	R26
	1OEN	R15	R27
	2OEN	R16	R28
Eight Channel(4)	DIR	R11	R30
	OEN	R9	R12

(1) One channel considering SN74AXC1T45 or SN74AVC1T45 or SN74LVC1T45
(2) Two channel considering SN74AVC2T45 or SN74LVC2T45
(3) Four channel considering SN74AXC4T245 or SN74AVC4T245
(4) Four channel considering SN74AXC8T245 or SN74AVC8T245 or SN74LVC8T245

1.2.4 SMB Connectors

The edge-mounted SMB connector option is provided for each of the channel versions on data I/O pins of A1 and B1, respectively, for high-speed operation. One pair of SMB connector is installed on the A1 and B1 data I/O pair of the 8-channel device option while the corresponding header pin has an uninstalled 0-Ω resistor R18 and R17. The data I/O pins A8, B8 also have the uninstalled SMB connector option with 0-Ω resistors to headers.

2 Board Layout

Figure 2-1 illustrates the EVM layout. Increase zoom level for clarity.

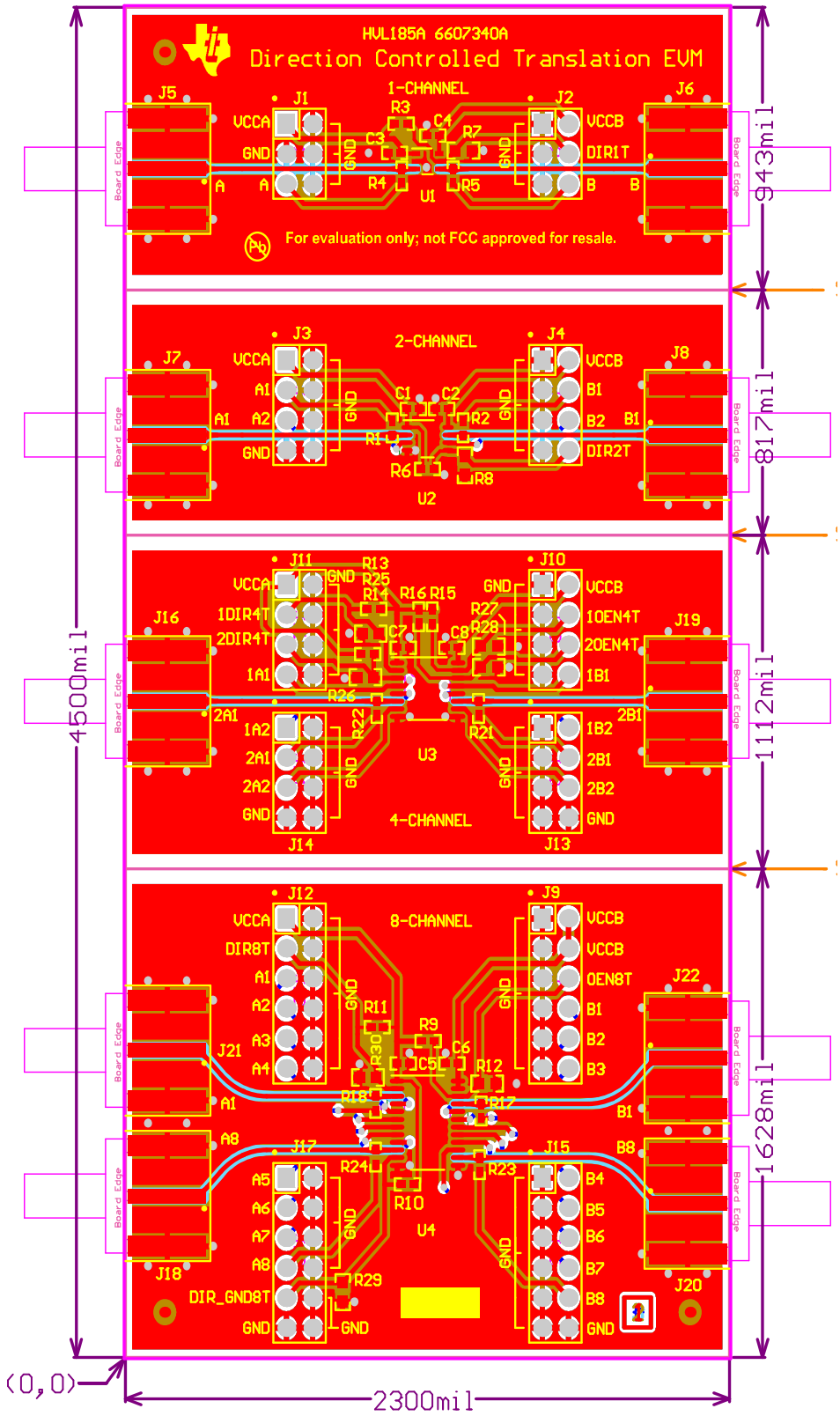

Figure 2-1. AVCLVCDIRCNTRL-EVM Layout

3 Schematic and Bill of Materials

3.1 Schematic

Figure 3-1 illustrates the EVM schematic. Increase the zoom level for clarity.

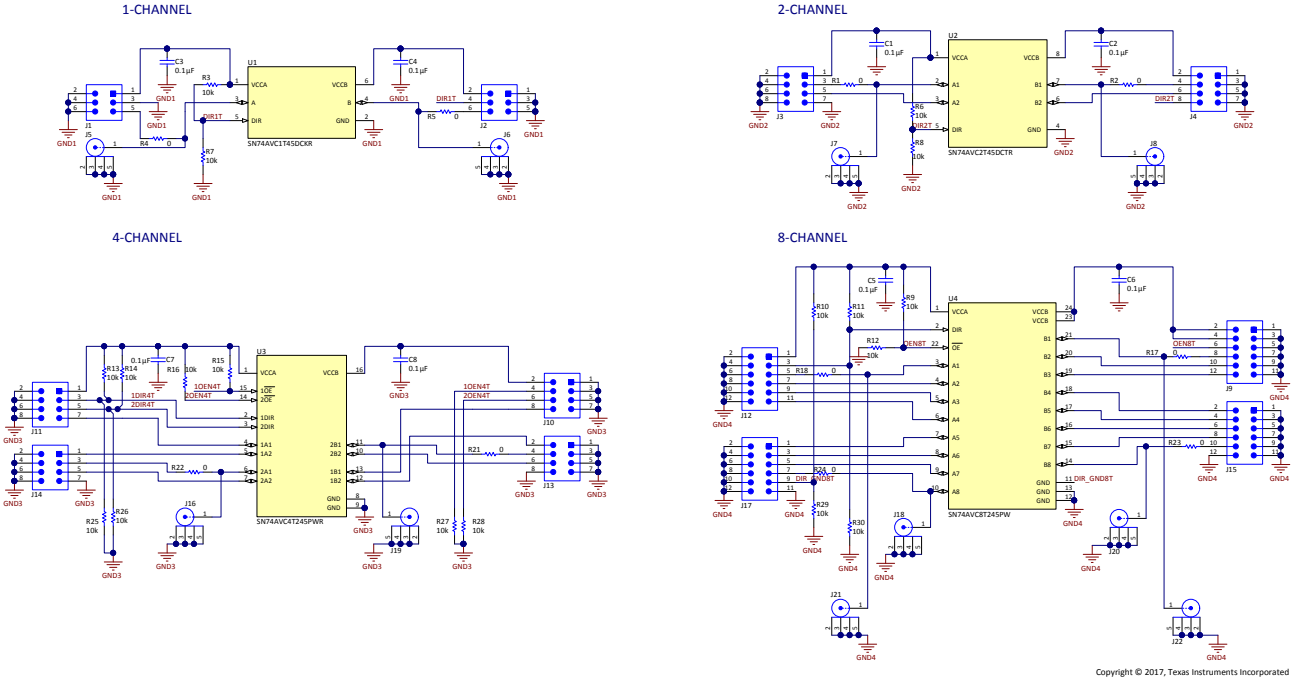

Figure 3-1. Generic AVCLVCDIRCNTRL-EVM Schematic

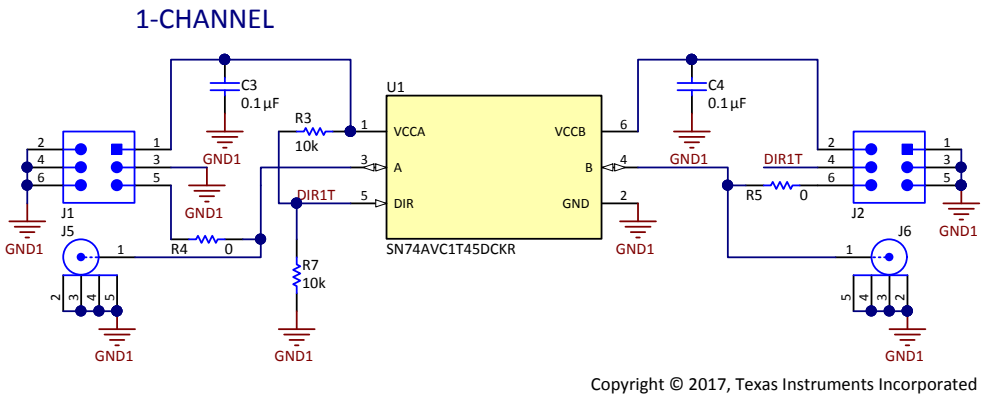

Figure 3-2. One Channel

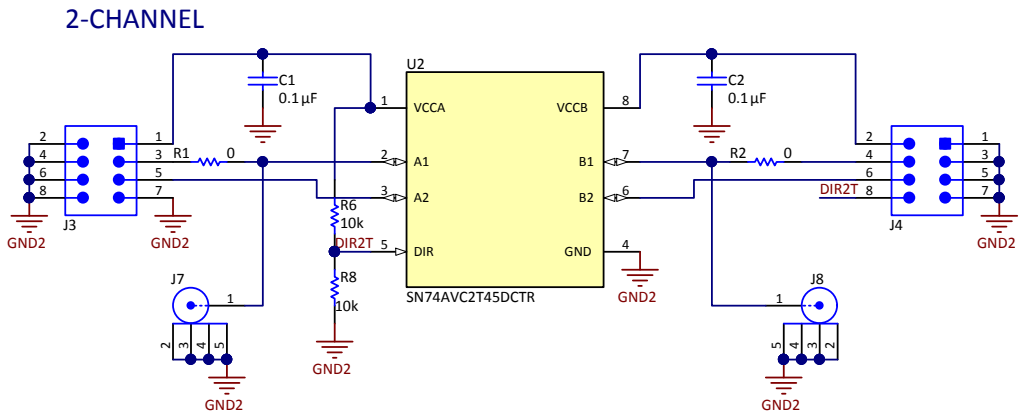

Figure 3-3. Two Channel

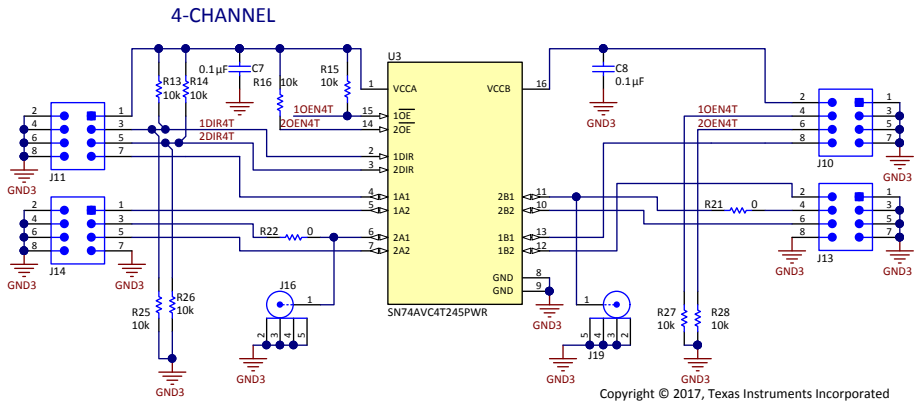

Figure 3-4. Four Channel

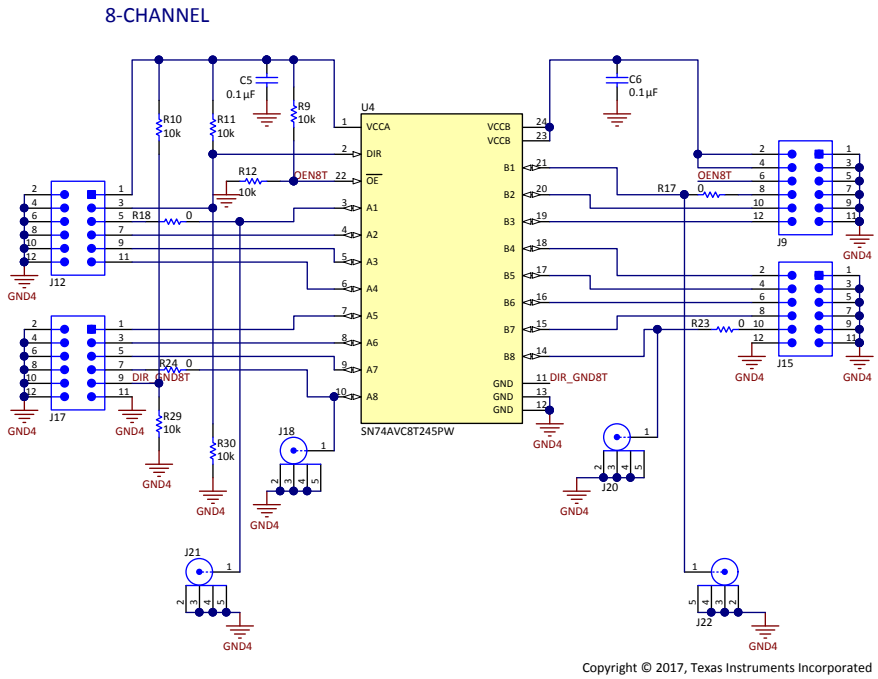

Figure 3-5. Eight Channel

3.2 Bill of Materials

Table 3-1 lists the EVM bill of materials.

Table 3-1. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		6607340	Any
C1, C2, C3, C4, C5, C6, C7, C8	8	0.1uF	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0402	0402	0402YC104KAT2A	AVX
J1, J2	2		Header, 100mil, 3x2, Gold, TH	3x2 Header	TSW-103-07-G-D	Samtec
J3, J4, J10, J11, J13, J14	6		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec
J9, J12, J15, J17	4		Header, 100mil, 6x2, Gold, TH	6x2 Header	TSW-106-07-G-D	Samtec
J21, J22	2		Connector, SMB Jack, End launch, SMT	SMB End launch Jack, SMT	131-3701-801	Emerson Network Power
R1, R2, R4, R5, R21, R22, R23, R24	8	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2GE0R00X	Panasonic
R3, R6, R9, R11, R13, R14, R15, R16	8	10k	RES, 10 k, 5%, 0.063 W, 0402	0402	CRCW040210K0JNED	Vishay-Dale
R29	1	10k	RES, 10 k, 5%, 0.1 W, 0603	0603	CRCW060310K0JNEA	Vishay-Dale
J5, J6, J7, J8, J16, J18, J19, J20	0		Connector, SMB Jack, End launch, SMT	SMB End launch Jack, SMT	131-3701-801	Emerson Network Power
R7, R8, R12, R25, R26, R27, R28, R30	0	10k	RES, 10 k, 5%, 0.1 W, 0603	0603	CRCW060310K0JNEA	Vishay-Dale
R17, R18	0	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2GE0R00X	Panasonic
R10	0	10k	RES, 10 k, 5%, 0.063 W, 0402	0402	CRCW040210K0JNED	Vishay-Dale
U1	0		Single-Bit Dual-Supply Bus Transceiver with Configurable Voltage-Level Shifting DCK0006A (SOT-6)	DCK0006A	SN74AVC1T45DCKR	Texas Instruments
U2	0		Dual-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation, DCT0008A (SSOP-8)	DCT0008A	SN74AVC2T45DCTR	Texas Instruments
U3	0		4-Bit Dual-Supply Bus Transceiver with Configurable Voltage-Level Shifting, PW0016A (TSSOP-16)	PW0016A	SN74AVC4T245PWR	Texas Instruments
U4	0		8-Bit Dual-Supply Bus Transceiver with Configurable Voltage-Level Shifting, PW0024A (TSSOP-24)	PW0024A	SN74AVC8T245PWR	Texas Instruments

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2019) to Revision B (July 2021) **Page**

- Updated the numbering format for tables, figures and cross-references throughout the document.....2

Changes from Revision * (August 2017) to Revision A (February 2019) **Page**

- Added AXC devices to the Features section and Supported Devices table.....2

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265