BLP05H9S500P

Power LDMOS transistor

Rev. 1 — 10 September 2019

AMPLEON

Product data sheet

1. Product profile

1.1 General description

500 W LDMOS power transistor for various applications such as ISM, RF plasma lighting and defrosting at frequencies from 423 MHz to 443 MHz.

Table 1. Typical performance

RF performance at V_{DS} = 50 V; I_{Dq} = 50 mA in a class-AB application circuit.

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	433	50	500	25.3	75
CW pulsed [1]	433	50	500	25.6	75.8

[1] t_p = 100 μs; δ = 10 %.

1.2 Features and benefits

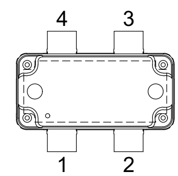
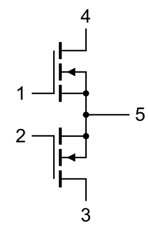
- High efficiency
- Easy power control
- Excellent ruggedness
- Integrated ESD protection
- Designed for ISM operation (423 MHz to 443 MHz)
- Excellent thermal stability
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for CW and pulsed CW applications in the 423 MHz to 443 MHz frequency range such as ISM, RF plasma lighting and defrosting

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	gate 2		 aaa-003574
2	gate 1		
3	drain 1		
4	drain 2		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP05H9S500P	-	plastic, heatsink small outline package; 4 leads (flat)	OMP-780-4F-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	108	V
V_{GS}	gate-source voltage	–6	+11	V
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature [1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C; P_L = 500 W	0.22	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.8 mA	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 180 mA	1.5	2.1	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	31	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 9 A	-	13	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 6.3 A	-	0.12	-	Ω

Table 7. RF characteristics

Test signal: CW pulsed (t_p = 100 μs; δ = 10 %); f = 443 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 500 W	24	25.2	-	dB
RL_{in}	input return loss	P_L = 500 W	-	−14.5	−9	dB
η_D	drain efficiency	P_L = 500 W	68	72	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLP05H9S500P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 50 mA; P_L = 500 W (CW).

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull Z_S and Z_L device impedances per section; I_{Dq} = 25 mA per section; V_{DS} = 50 V; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]
(MHz)	(Ω)	(Ω)
433	1.3 – 2.1j	2.8 + 2.4j

[1] Z_S and Z_L defined in Figure 1.

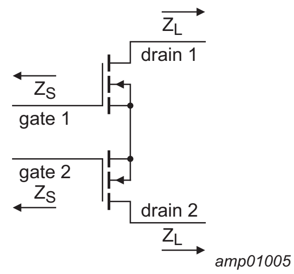
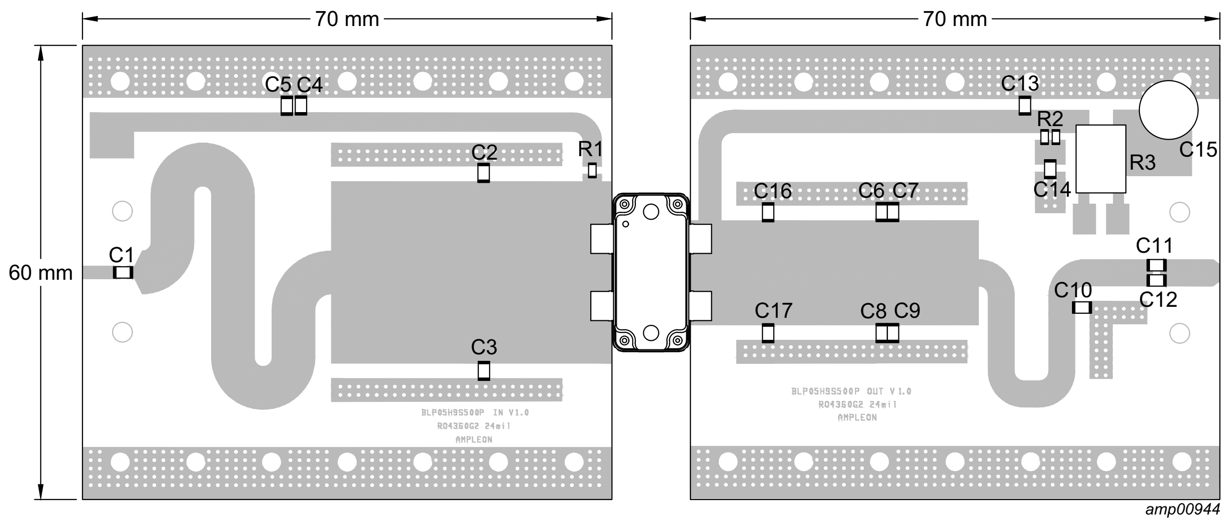


Fig 1. Definition of transistor impedance

7.3 Application circuit



Printed-Circuit Board (PCB): Rogers RO4360G2; thickness = 0.610 mm; ε_r = 6.15.

See Table 9 for a list of components.

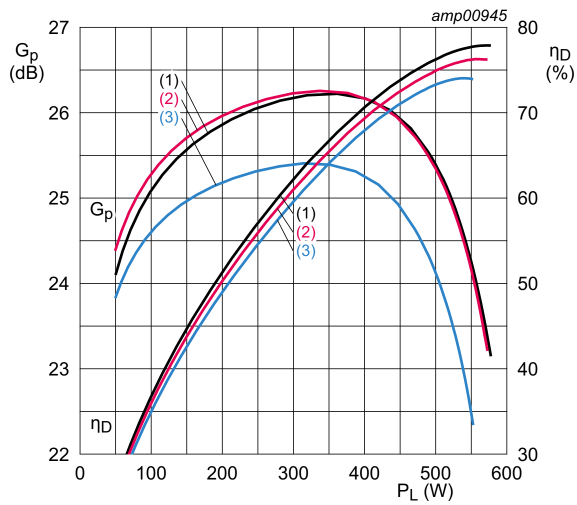
Fig 2. Component layout for class-AB application circuit

Table 9. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1, C4, C11, C12, C13	multilayer ceramic chip capacitor	270 pF	ATC800B
C2, C3	multilayer ceramic chip capacitor	75 pF	ATC800B
C5, C14	multilayer ceramic chip capacitor	4.7 μF, 100V	C3225X7S2A475K200AE
C6, C8	multilayer ceramic chip capacitor	27 pF	ATC800B
C7, C9	multilayer ceramic chip capacitor	18 pF	ATC800B
C10	multilayer ceramic chip capacitor	12 pF	ATC800B
C15	electrolytic capacitor	4.7 μF, 63 V	MAL203858471E3
C16, C17	multilayer ceramic chip capacitor	16 pF	ATC800B
R1	chip resistor	10 Ω	0806
R2, R4	chip resistor	9.1 Ω	1206
R3	shunt resistor	0.01 Ω	Ohmite: FC4L110R010FER

7.4 Graphical data



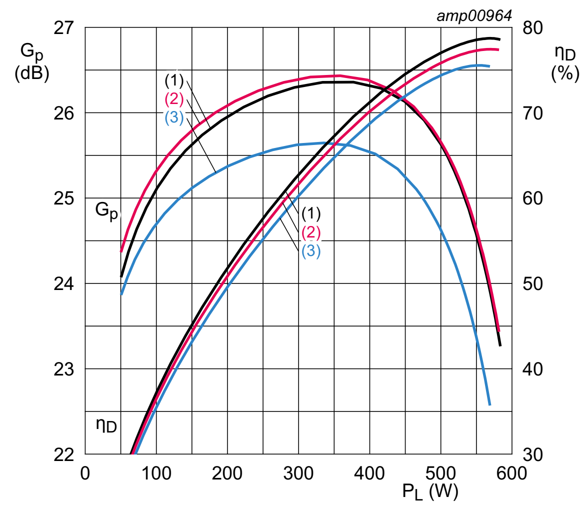
V_{DS} = 50 V; I_{Dq} = 50 mA; CW.

(1) f = 423 MHz

(2) f = 433 MHz

(3) f = 443 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



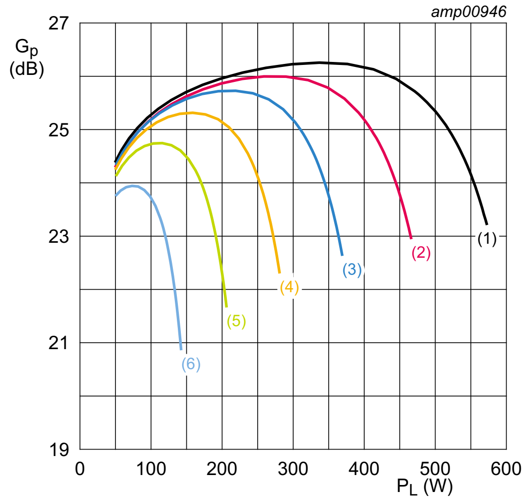
V_{DS} = 50 V; I_{Dq} = 50 mA; CW pulsed; t_p = 100 μs; δ = 10 %.

(1) f = 423 MHz

(2) f = 433 MHz

(3) f = 443 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



f = 433 MHz; I_{Dq} = 50 mA; CW.

(1) V_{DS} = 50 V

(2) V_{DS} = 45 V

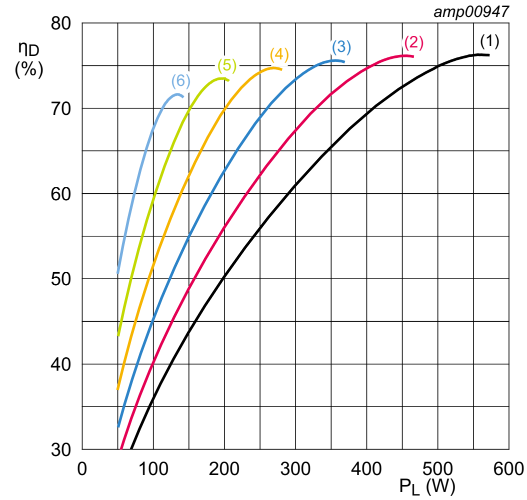
(3) V_{DS} = 40 V

(4) V_{DS} = 35 V

(5) V_{DS} = 30 V

(6) V_{DS} = 25 V

Fig 5. Power gain as a function of output power; typical values



f = 433 MHz; I_{Dq} = 50 mA; CW.

(1) V_{DS} = 50 V

(2) V_{DS} = 45 V

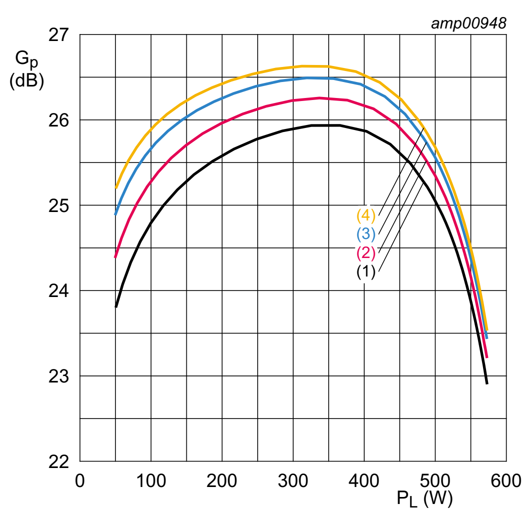
(3) V_{DS} = 40 V

(4) V_{DS} = 35 V

(5) V_{DS} = 30 V

(6) V_{DS} = 25 V

Fig 6. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; f = 433 MHz; CW.

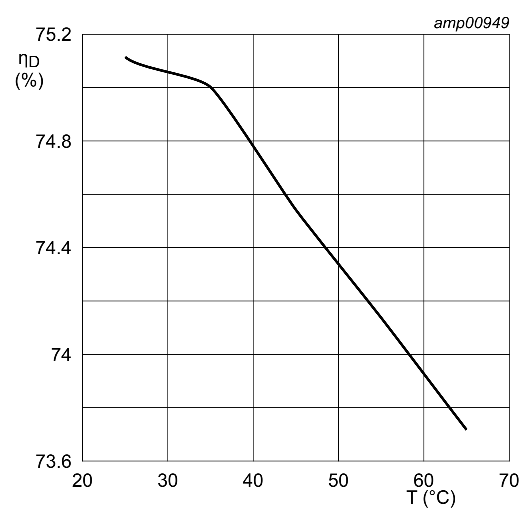
(1) I_{Dq} = 20 mA

(2) I_{Dq} = 50 mA

(3) I_{Dq} = 100 mA

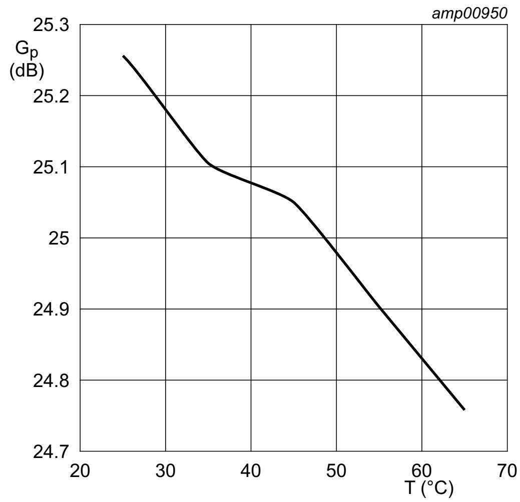
(4) I_{Dq} = 150 mA

Fig 7. Power gain as a function of output power; typical values



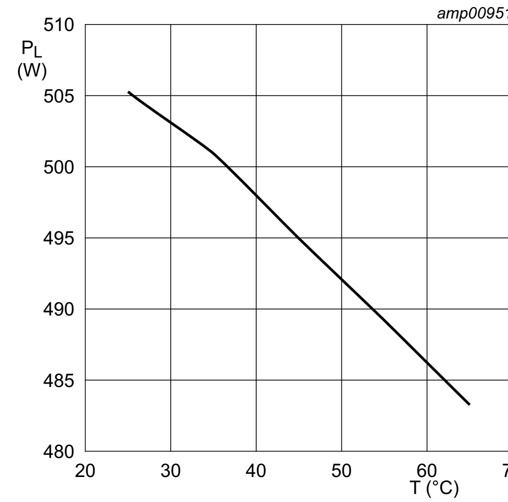
V_{DS} = 50 V; I_{Dq} = 50 mA; f = 433 MHz; CW; at $P_{L(1dB)}$.

Fig 8. Drain efficiency as a function of temperature; typical values



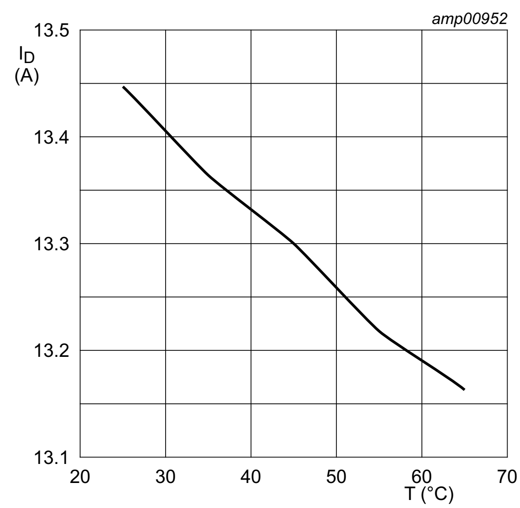
V_{DS} = 50 V; I_{Dq} = 50 mA; f = 433 MHz; CW; at $P_{L(1dB)}$.

Fig 9. Power gain as a function of temperature; typical values



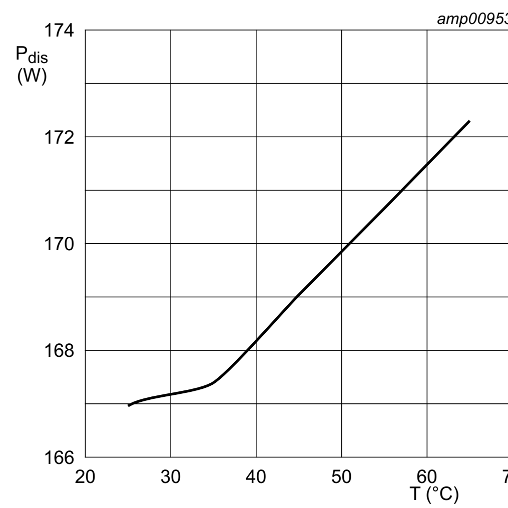
V_{DS} = 50 V; I_{Dq} = 50 mA; f = 433 MHz; CW; at $P_{L(1dB)}$.

Fig 10. Output power as a function of temperature; typical values



V_{DS} = 50 V; I_{Dq} = 50 mA; f = 433 MHz; CW; at $P_{L(1dB)}$.

Fig 11. Drain current as a function of temperature; typical values

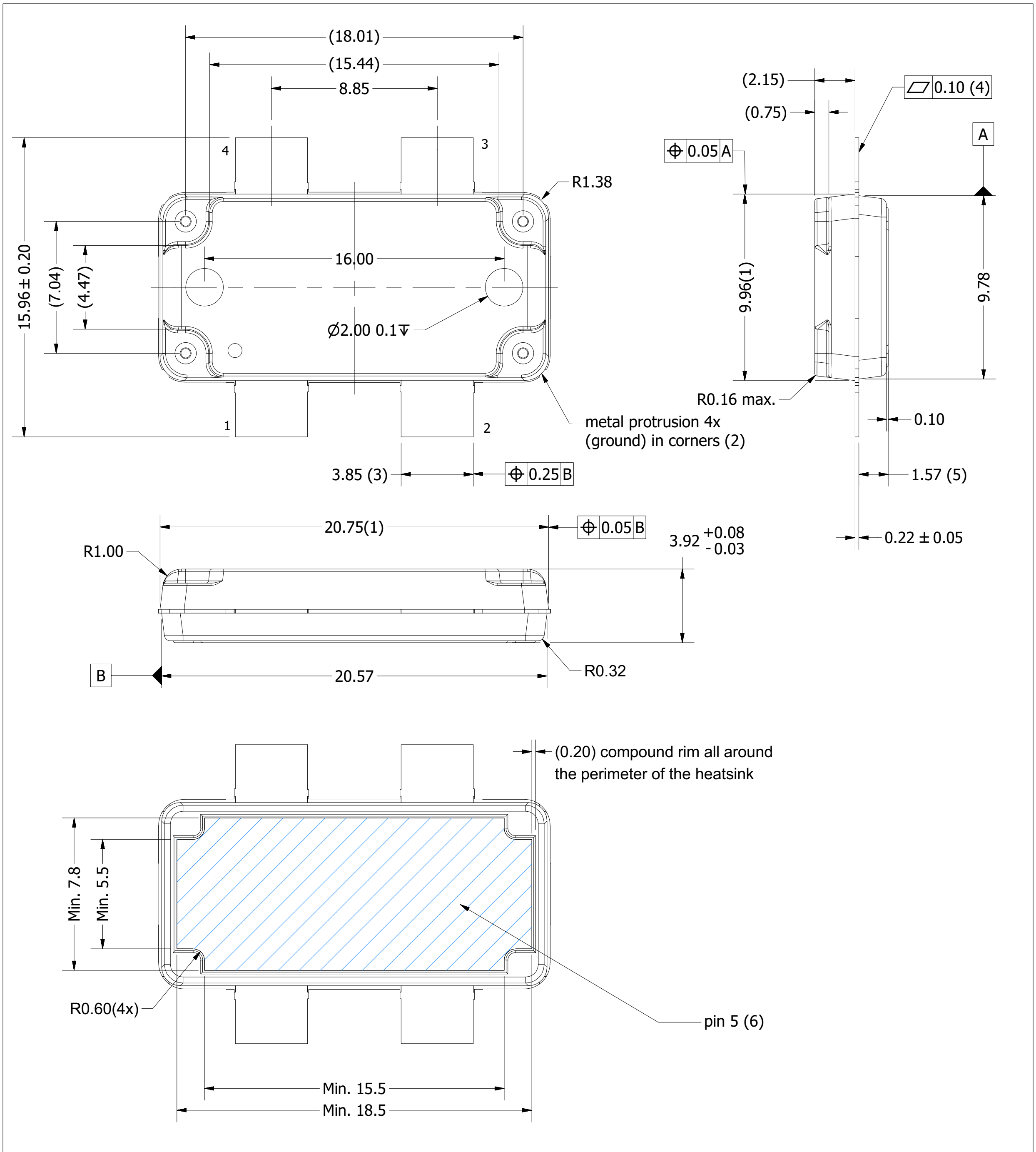


V_{DS} = 50 V; I_{Dq} = 50 mA; f = 433 MHz; CW; at $P_{L(1dB)}$.

Fig 12. Power dissipation as a function of temperature; typical values

8. Package outline

OMP-780-4F-1

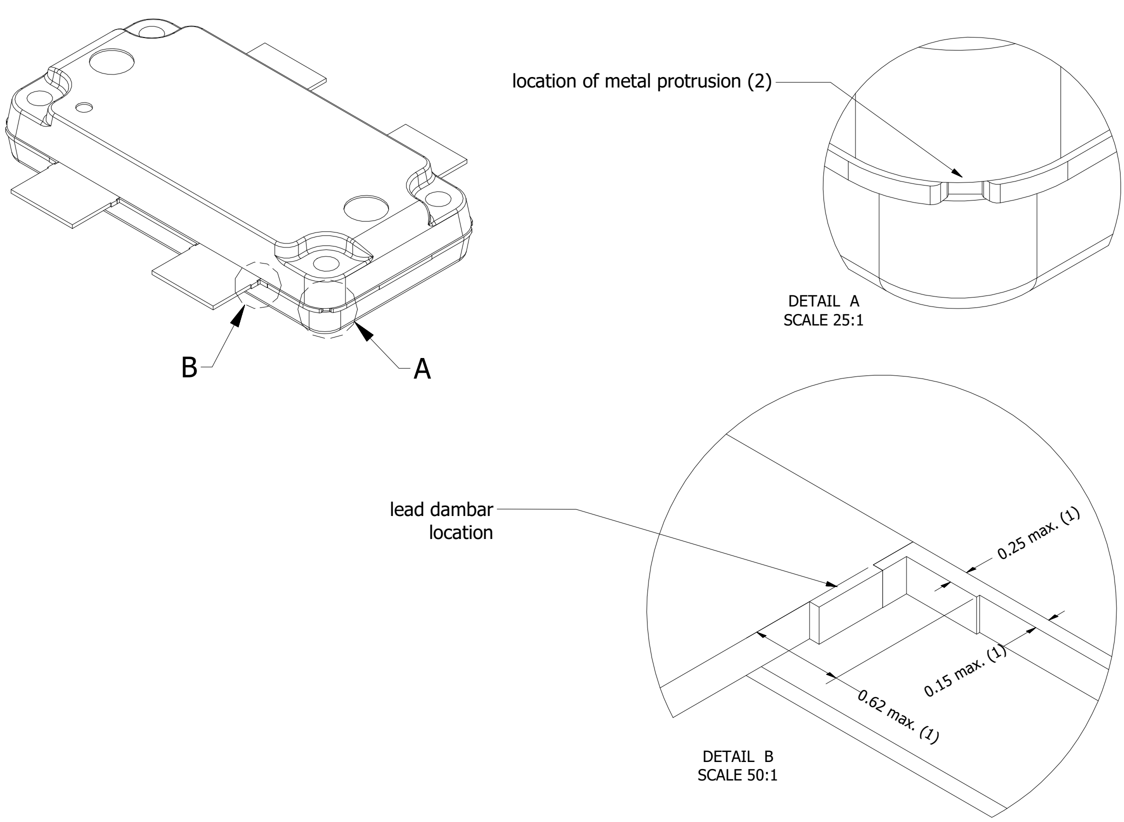


Package outline drawing: OMP-780-4F-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 3/1/2018
		Third angle projection	Sheet 1 of 2

Fig 13. Package outline OMP-780-4F-1 (sheet 1 of 2)

OMP-780-4F-1

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. All areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and max. 0.62 mm in length. At all other areas the mold protrusion is maximum 0.15 mm per side. See also detail B.
(2)	The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A).
(3)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(4)	The lead coplanarity over all leads is 0.1 mm maximum.
(5)	Dimension is measured 0.5 mm from the edge of the top package body.
(6)	The hatched area indicates the exposed metal heatsink.
(7)	The leads and exposed heatsink are plated with matte Tin (Sn).



Package outline drawing:	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 3/1/2018
OMP-780-4F-1		Third angle projection	Sheet 2 of 2

Fig 14. Package outline OMP-780-4F-1 (sheet 2 of 2)

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP05H9S500P v.1	20190910	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contents

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